Abstract Of The Disclosure

A solid-state image sensor has a readout architecture that incorporates charge multiplier cells into a horizontal register of a CCD image sensor, and includes a first CCD register adjacent to at least a second CCD register and coupled to the said first register through a charge overflow barrier. A high Dynamic Range readout system results in which the DR is not restricted by the voltage swing limitations on the charge detection node. As the charge is multiplied, the horizontal register structure increases in width and more charge multiplication gates are added per stage. A charge overflow region follows the charge multiplier. In this region the amount of charge that exceeds a certain predetermined threshold is split off into another register. A detection node that has different conversion sensitivity may terminate this register. The process of charge overflow and splitting off may continue for more than two steps.